

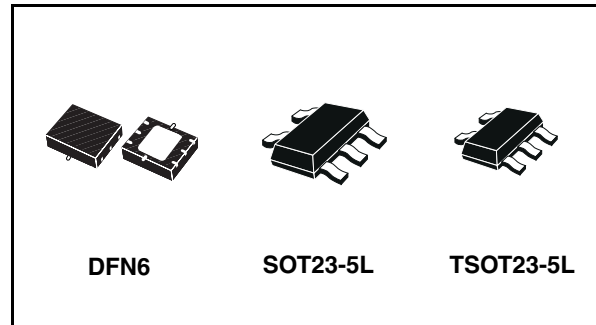


# LDS3985xx

Ultra low drop-low noise BiCMOS 300 mA volt. reg.  
for use with very low ESR output capacitor

## Features

- Input voltage from 2.5 V to 6 V
- Stable with low ESR ceramic capacitors
- Ultra low dropout voltage (150 mV typ. at 300 mA load, 0.4 mV typ. at 1 mA load)
- Very low quiescent current (85  $\mu$ A typ. at no load, 200  $\mu$ A typ. at 300 mA load; max 1.5  $\mu$ A in OFF mode)
- Guaranteed output current up to 300 mA
- Wide range of output voltage: from 1.25 V to 5.0 V
- Fast turn-on time: typ. 240  $\mu$ s [ $C_O = 2.2 \mu$ F,  $C_{BYP} = 33$  nF and  $I_O = 1$  mA]
- Logic-controlled electronic shutdown
- Internal current and thermal limit
- Output low noise voltage 30  $\mu$ V<sub>RMS</sub> over 10 Hz to 100 kHz
- SVR of 55 dB at 1 kHz, 50 dB at 10 kHz
- Temperature range: -40 °C to 125 °C



It is stable with ceramic and high quality tantalum capacitor. The ultra low drop voltage, low quiescent current and low noise makes it suitable for low power applications and in battery powered systems. Regulator ground current increases only slightly in dropout, further prolonging the battery life. Shutdown logic control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. Typical applications are in mobile phone and similar battery powered wireless systems, portable information appliances.

## Description

The LDS3985 provides up to 300 mA, from 2.5 V to 6 V input voltage.

Table 1. Device summary

Part number	Output voltage
LDS3985XX15	1.5 V
LDS3985XX18	1.8 V
LDS3985XX25	2.5 V
LDS3985XX28	2.8 V
LDS3985XX30	3.0 V
LDS3985XX33	3.3 V

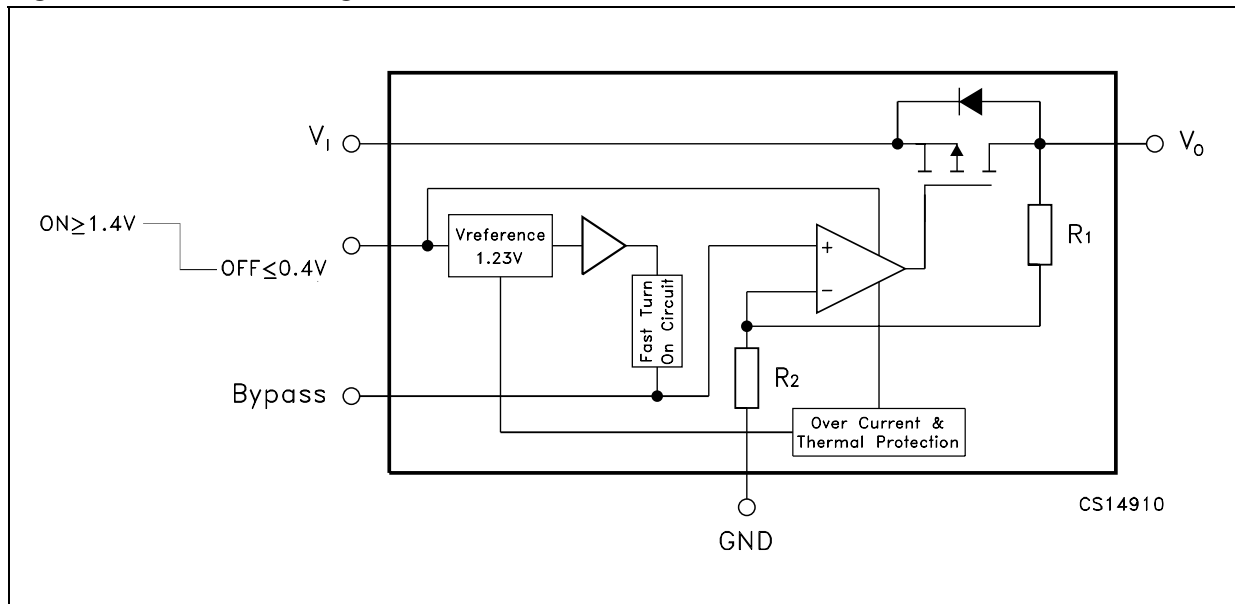
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# 1 Diagram

Figure 1. Schematic diagram



## 2 Pin configuration

Figure 2. Pin connections (top view for SOT and TSOT, top through view for DFN6)

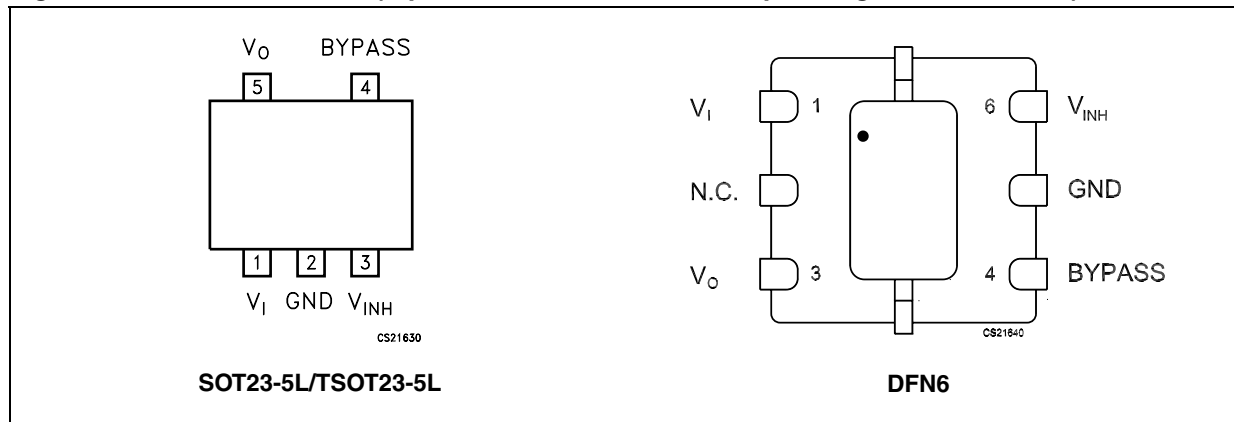
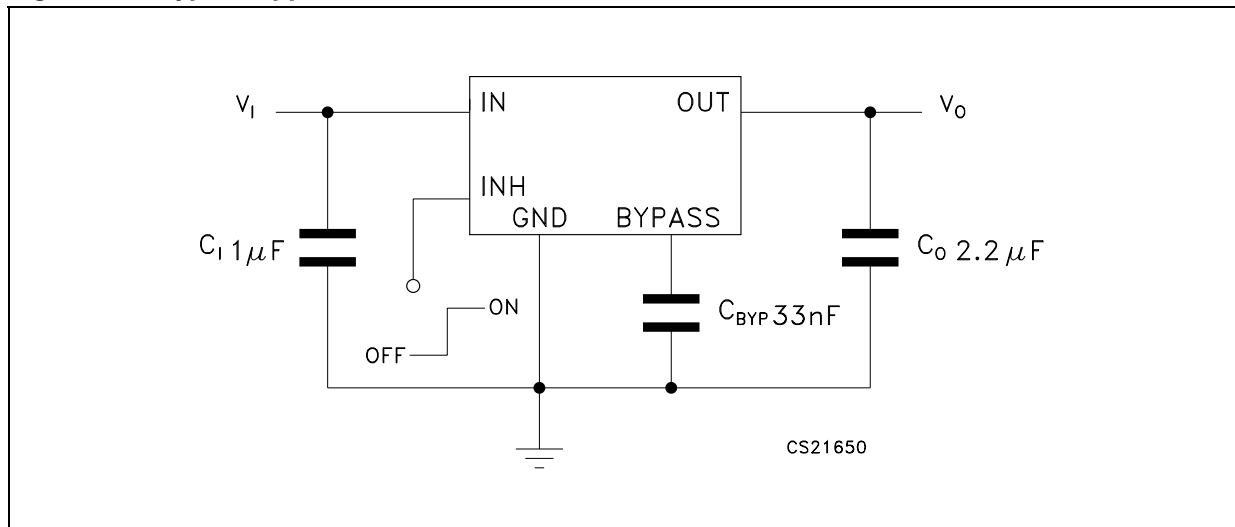


Table 2. Pin description

Pin n° for SOT23-5L/TSOT23-5L	Pin n° for DFN6	Symbol	Name and function
1	1	$V_I$	Input voltage of the LDO
2	5	GND	Common ground
3	6	$V_{INH}$	Inhibit input voltage: ON MODE when $V_{INH} \geq 1.2$ V, OFF MODE when $V_{INH} \leq 0.4$ V (Do not leave floating, not internally pulled down/up)
4	4	BYPASS	Bypass pin: connect an external capacitor (usually 10 nF) to minimize noise voltage
5	3	$V_O$	Output voltage of the LDO
-	2	N.C.	Not connect

### 3 Typical application

Figure 3. Typical application circuit



## 4 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_I$	DC input voltage	-0.3 to 6 <sup>(1)</sup>	V
$V_O$	DC output voltage	-0.3 to $V_I+0.3$	V
$V_{INH}$	INHIBIT input voltage	-0.3 to $V_I+0.3$	V
$I_O$	Output current	Internally limited	
$P_D$	Power dissipation	Internally limited	
$T_{STG}$	Storage temperature range	-65 to 150	°C
$T_{OP}$	Operating junction temperature range	-40 to 125	°C

1. The input pin is able to withstand non repetitive spike of 6.5 V for 200 ms.

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.*

**Table 4. Thermal data**

Symbol	Parameter	SOT23-5L/ TSOT23	DFN6	Unit
$R_{thJC}$	Thermal resistance junction-case	81	10	°C/W
$R_{thJA}$	Thermal resistance junction-ambient	255	55	°C/W

## 5 Electrical characteristics

**Table 5. Electrical characteristics for LDS3985** ( $T_J = 25^\circ\text{C}$ ,  $V_I = V_{O(\text{NOM})} + 0.5\text{ V}$ ,  $C_I = 1\ \mu\text{F}$ ,  $C_O = 2.2\ \mu\text{F}$ ,  $C_{\text{BYP}} = 33\ \text{nF}$ ,  $I_O = 1\ \text{mA}$ ,  $V_{\text{INH}} = 1.4\ \text{V}$ , unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_I$	Operating input voltage		2.5		6	V
$V_O$	Output voltage < 2.5V	$I_O = 1\ \text{mA}$	-50		50	mV
		$T_J = -40\ \text{to}\ 125^\circ\text{C}$	-75		75	
$V_O$	Output voltage $\geq 2.5\text{V}$	$I_O = 1\ \text{mA}$	-2		2	% of $V_{O(\text{NOM})}$
		$T_J = -40\ \text{to}\ 125^\circ\text{C}$	-3		3	
$\Delta V_O$	Line regulation (1)	$V_I = V_{O(\text{NOM})} + 0.5\ \text{to}\ 6\ \text{V}$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$	-0.1		0.1	% / V
		$V_O = 4.7\ \text{to}\ 5\ \text{V}$	-0.19		0.19	
$\Delta V_O$	Load regulation	$I_O = 1\ \text{mA}\ \text{to}\ 300\ \text{mA}$ , $V_O \leq 2.5\text{V}$ $T_J = -40\ \text{to}\ 125^\circ\text{C}$		0.005	0.01	% / mA
$\Delta V_O$	Load regulation	$I_O = 1\ \text{mA}\ \text{to}\ 300\ \text{mA}$ , $V_O \geq 2.5\ \text{V}$ $T_J = -40\ \text{to}\ 125^\circ\text{C}$		0.0008	0.004	% / mA
$\Delta V_O$	Output AC line regulation (2)	$V_I = V_{O(\text{NOM})} + 1\ \text{V}$ , $I_O = 300\ \text{mA}$ , $t_R = t_F = 30\ \mu\text{s}$		5		mV <sub>PP</sub>
$I_Q$	Quiescent current ON MODE: $V_{\text{INH}} = 1.24\text{V}$	$I_O = 0$		85		$\mu\text{A}$
		$I_O = 0$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$			150	
		$I_O = 0\ \text{to}\ 300\ \text{mA}$		200		
		$I_O = 0\ \text{to}\ 300\ \text{mA}$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$			300	
	OFF MODE: $V_{\text{INH}} = 0.4\text{V}$		0.003			
		$T_J = -40\ \text{to}\ 125^\circ\text{C}$			1.5	
$V_{\text{DROP}}$	Dropout voltage (3)	$I_O = 1\ \text{mA}$		0.4		mV
		$I_O = 1\ \text{mA}$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$			2	
		$I_O = 150\ \text{mA}$		60		
		$I_O = 150\ \text{mA}$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$			100	
		$I_O = 300\ \text{mA}$		150		
		$I_O = 300\ \text{mA}$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$			250	
$I_{\text{SC}}$	Short circuit current	$R_L = 0$		600		mA
SVR	Supply voltage rejection	$V_I = V_{O(\text{NOM})} + 0.25\ \text{V} \pm V_{\text{RIPPLE}} = 0.1\ \text{V}$ , $I_O = 50\ \text{mA}$ For $V_{O(\text{NOM})} < 2.5\ \text{V}$ , $V_I = 2.55\ \text{V}$	$f = 1\ \text{kHz}$		55	dB
			$f = 10\ \text{kHz}$		50	
$I_{O(\text{PK})}$	Peak output current	$V_O \geq V_{O(\text{NOM})} - 5\%$	300	550		mA
$V_{\text{INH}}$	Inhibit input logic Low	$V_I = 2.5\ \text{V}\ \text{to}\ 6\ \text{V}$ , $T_J = -40\ \text{to}\ 125^\circ\text{C}$			0.4	V
	Inhibit input logic High		1.4			
$I_{\text{INH}}$	Inhibit input current	$V_{\text{INH}} = 0.4\ \text{V}$ , $V_I = 6\ \text{V}$		$\pm 1$		nA

**Table 5. Electrical characteristics for LDS3985 (continued)** ( $T_J = 25^\circ\text{C}$ ,  $V_I = V_{O(\text{NOM})} + 0.5\text{ V}$ ,  $C_I = 1\ \mu\text{F}$ ,  $C_O = 2.2\ \mu\text{F}$ ,  $C_{\text{BYP}} = 33\ \text{nF}$ ,  $I_O = 1\ \text{mA}$ ,  $V_{\text{INH}} = 1.4\ \text{V}$ , unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
eN	Output noise voltage	$B_W = 10\ \text{Hz to } 100\ \text{kHz}$ , $C_O = 2.2\ \mu\text{F}$		30		$\mu\text{V}_{\text{RMS}}$
$t_{\text{ON}}$	Turn On time <sup>(4)</sup>	$C_{\text{BYP}} = 33\ \text{nF}$		240		$\mu\text{s}$
$T_{\text{SHDN}}$	Thermal shutdown	<sup>(5)</sup>		160		$^\circ\text{C}$
$C_O$	Output capacitor	Capacitance	2.2		22	$\mu\text{F}$
		ESR	5		5000	$\text{m}\Omega$

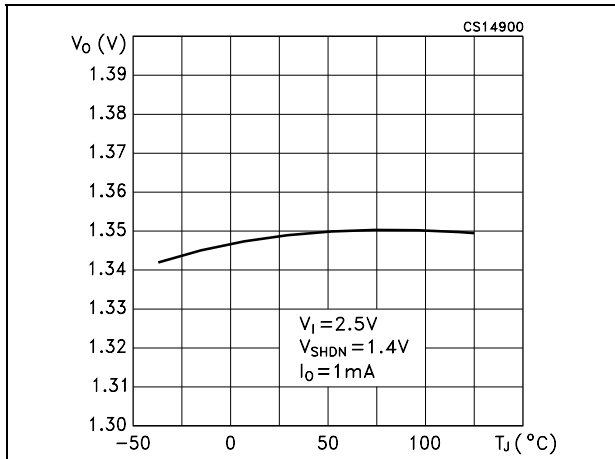
1. For  $V_{O(\text{NOM})} < 2\ \text{V}$ ,  $V_I = 2.5\ \text{V}$
2. For  $V_{O(\text{NOM})} = 1.25\ \text{V}$ ,  $V_I = 2.5\ \text{V}$
3. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for input voltages below 2.5 V
4. Turn -on time is time measured between the enable input just exceeding  $V_{\text{INH}}$  high value and the output voltage just reaching 95 % of its nominal value
5. Typical thermal protection hysteresis is  $20\ ^\circ\text{C}$



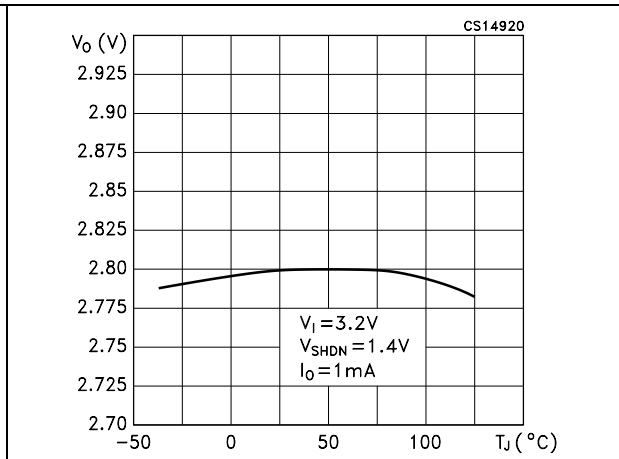
# 6 Typical performance characteristics

( $T_J = 25\text{ }^\circ\text{C}$ ,  $V_I = V_{O(NOM)} + 0.5\text{ V}$ ,  $C_I = 1\text{ }\mu\text{F}$ ,  $C_O = 2.2\text{ }\mu\text{F}$ ,  $C_{BYP} = 33\text{ nF}$ ,  $I_O = 1\text{ mA}$ ,  $V_{INH} = 1.4\text{ V}$ , unless otherwise specified)

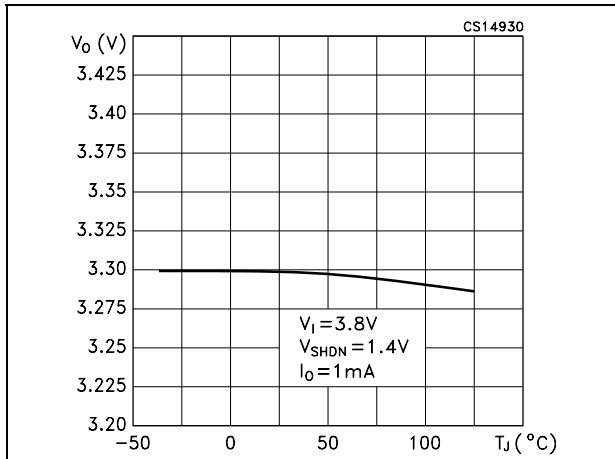
**Figure 4. Output voltage vs temperature**



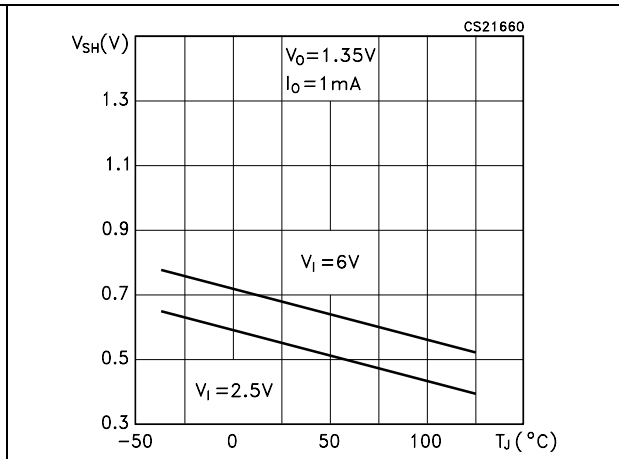
**Figure 5. Output voltage vs temperature**



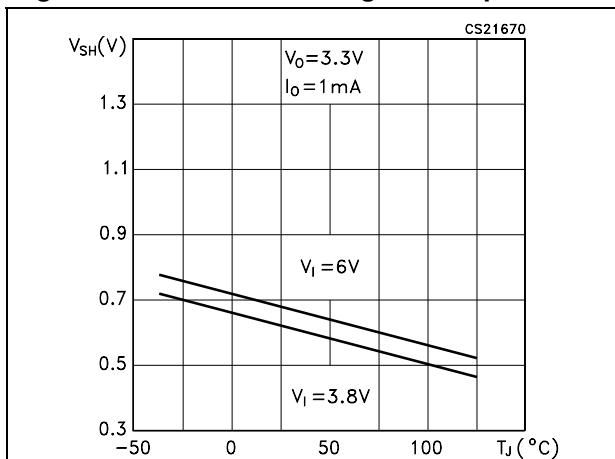
**Figure 6. Output voltage vs temperature**



**Figure 7. Shutdown voltage vs temperature**



**Figure 8. Shutdown voltage vs temperature**



**Figure 9. Line regulation vs temperature**

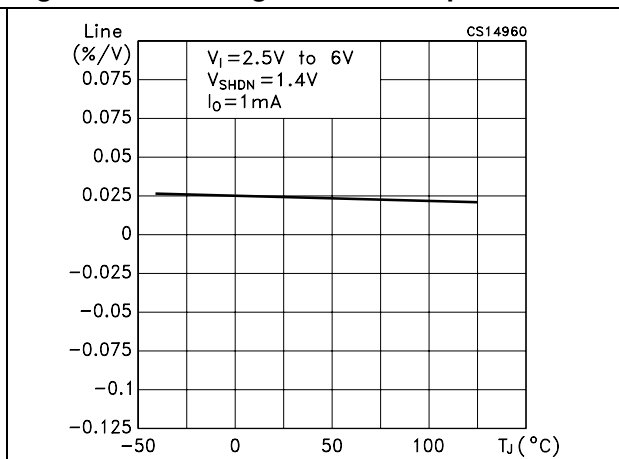


Figure 10. Line regulation vs temperature

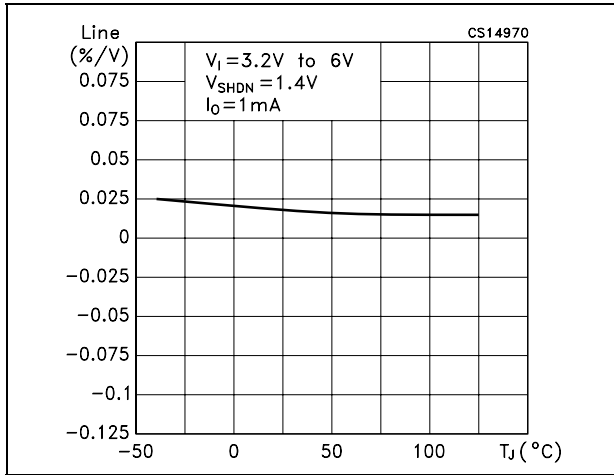


Figure 11. Line regulation vs temperature

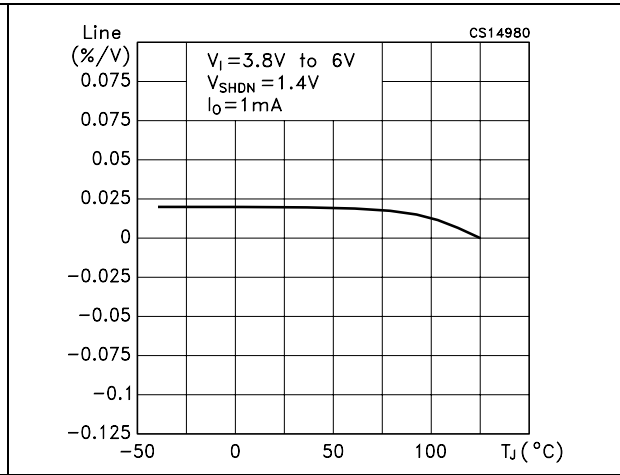


Figure 12. Quiescent current vs temperature

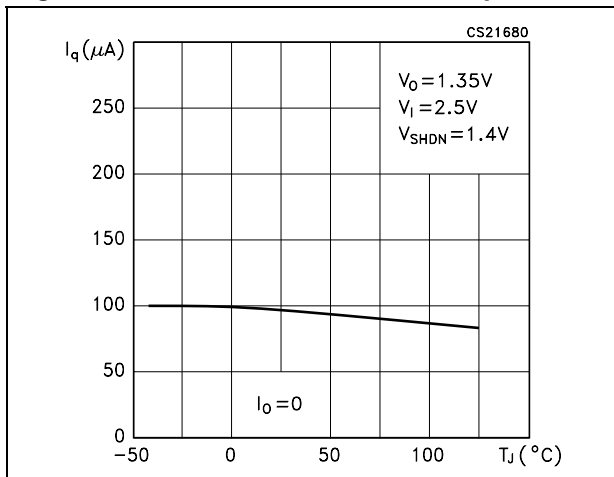


Figure 13. Quiescent current vs temperature

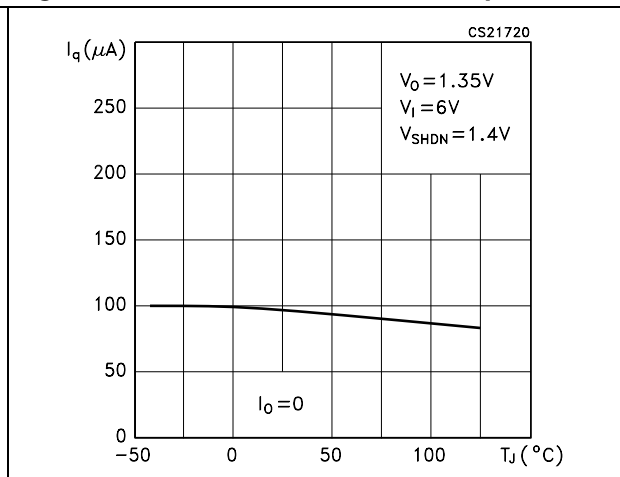


Figure 14. Quiescent current vs temperature

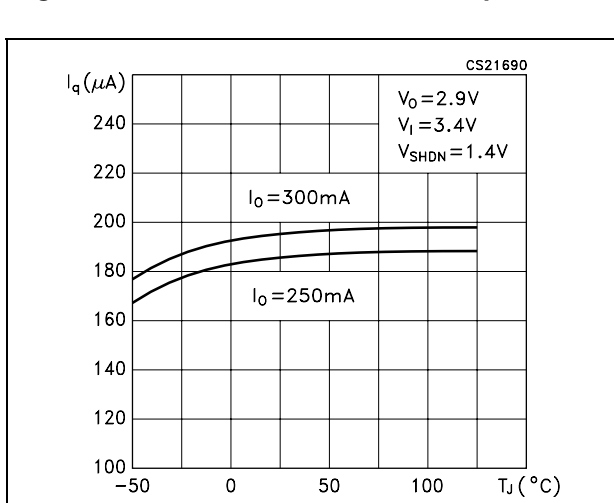


Figure 15. Supply voltage rejection vs frequency

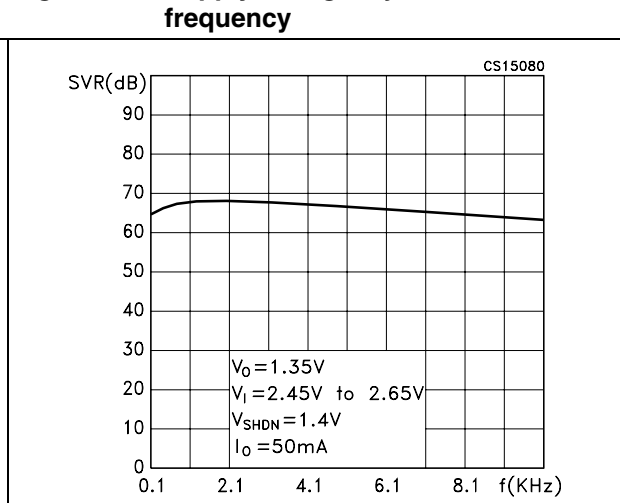


Figure 16. Dropout voltage vs temperature

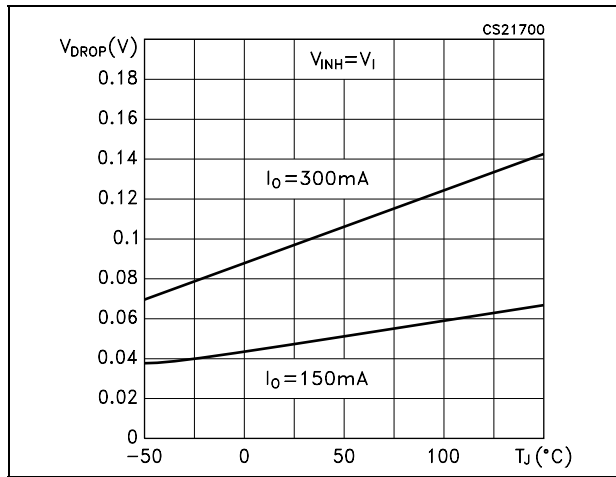


Figure 17. Dropout voltage vs output current

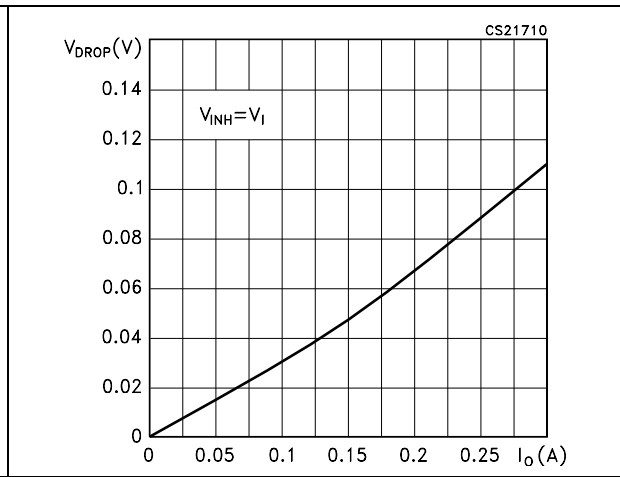
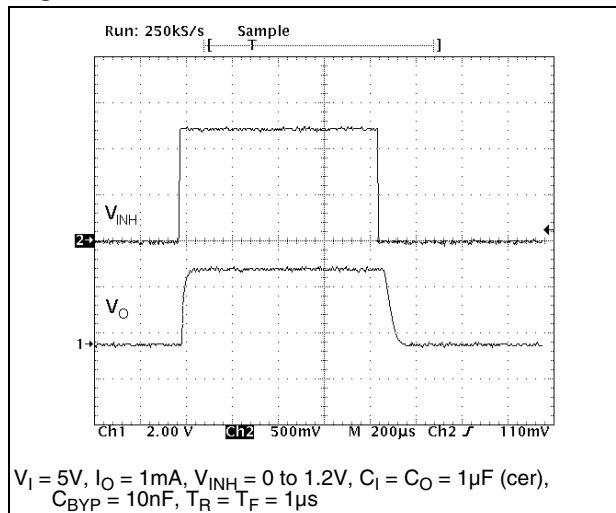


Figure 18. Inhibit transient

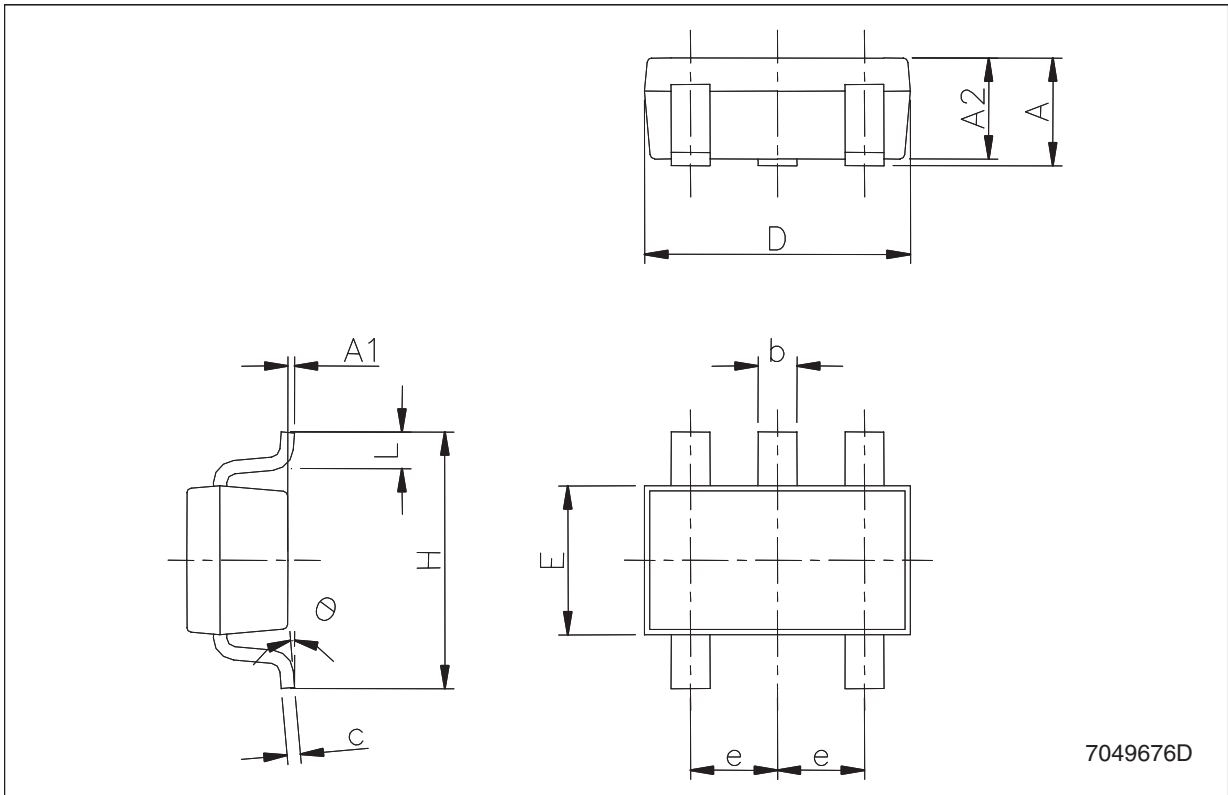


## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

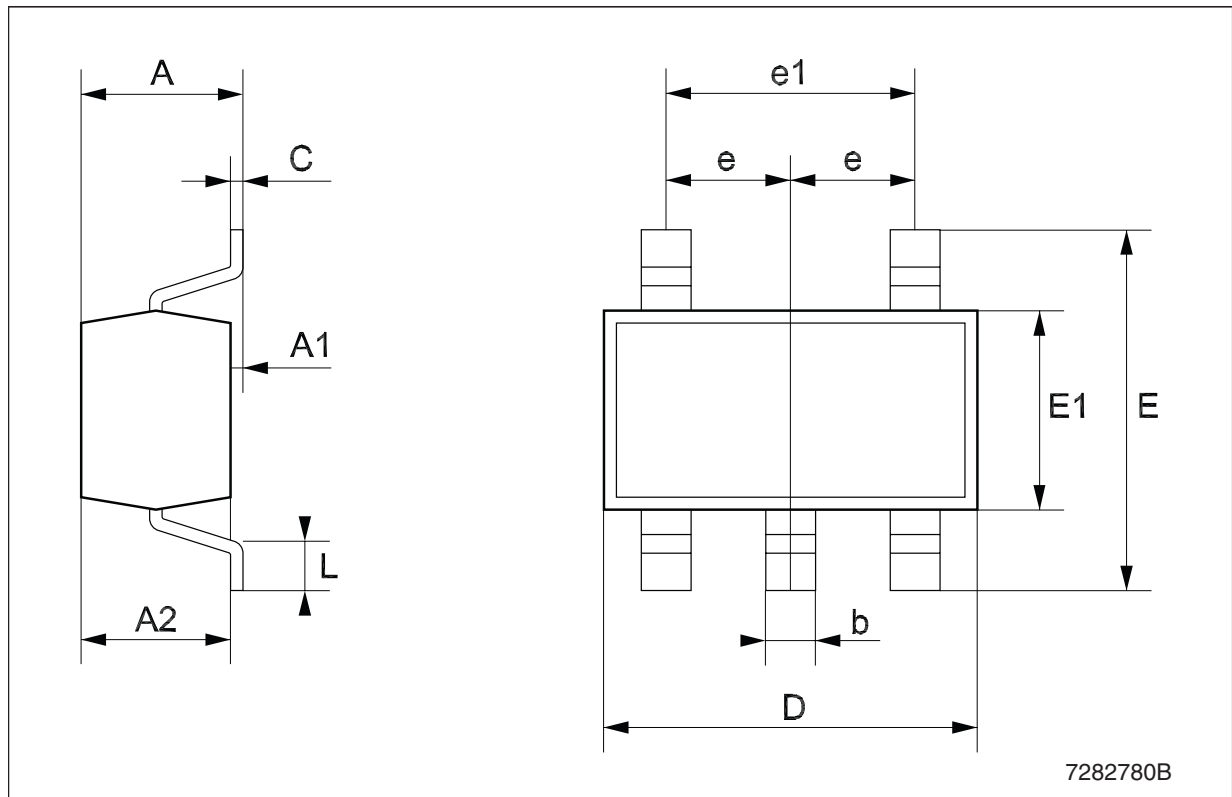
**SOT23-5L mechanical data**

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



**TSOT23-5L mechanical data**

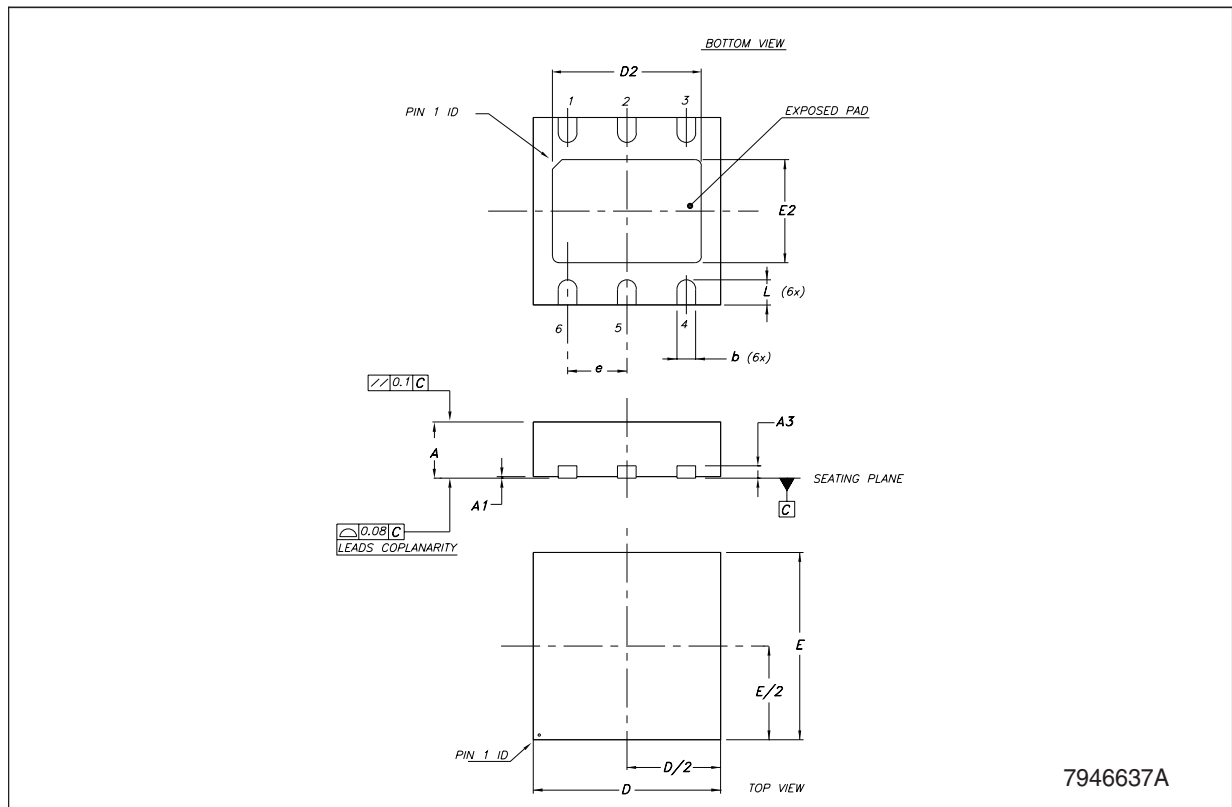
Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			43.3
A1	0		0.1			3.9
A2	0.7		1.0	27.6		39.4
b	0.3		0.5	11.8		19.7
C	0.08		0.2	3.1		7.9
D		2.9			114.2	
E		2.8			110.2	
E1		1.6			63.0	
e		0.95			37.4	
e1		1.9			74.8	
L	0.3		0.6	11.8		23.6



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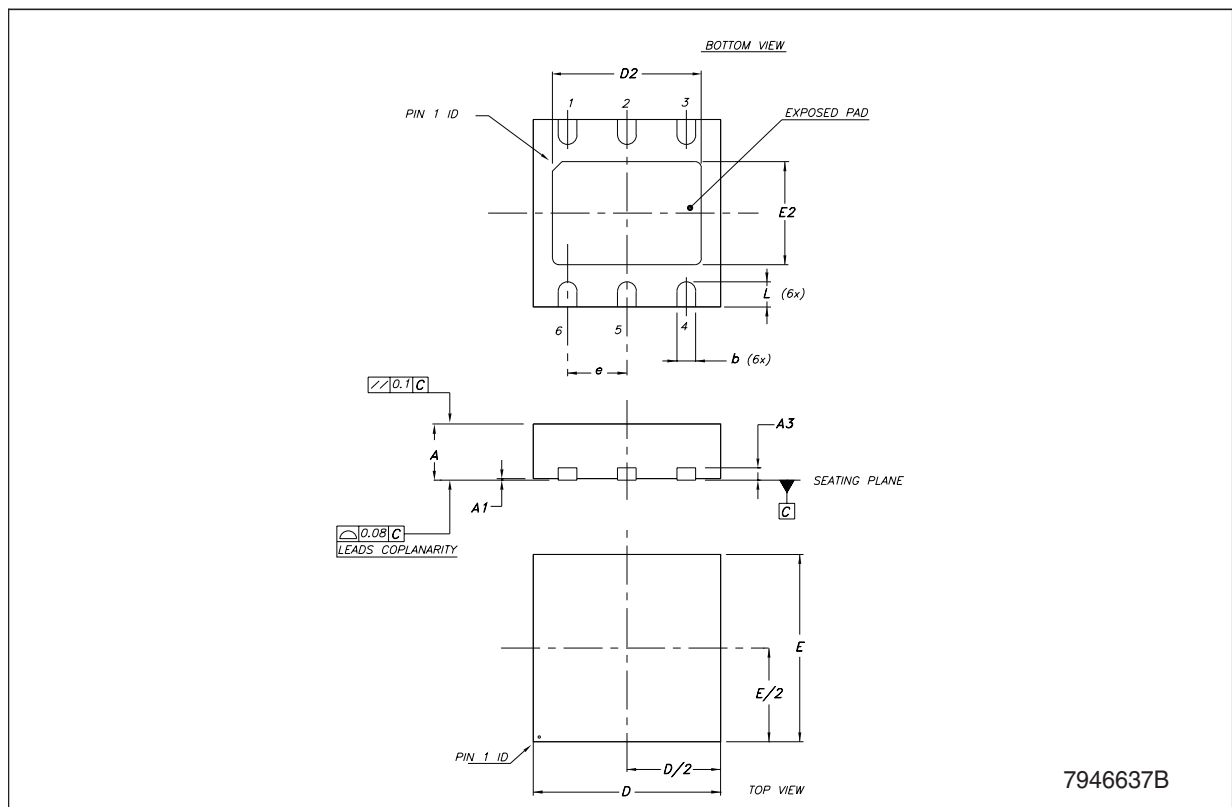
**DFN6 (3x3 mm) mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23	0.30	0.38	0.009	0.012	0.015
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23	2.38	2.48	0.088	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50	1.65	1.75	0.059	0.065	0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020



**DFN6D (3x3 mm) mechanical data**

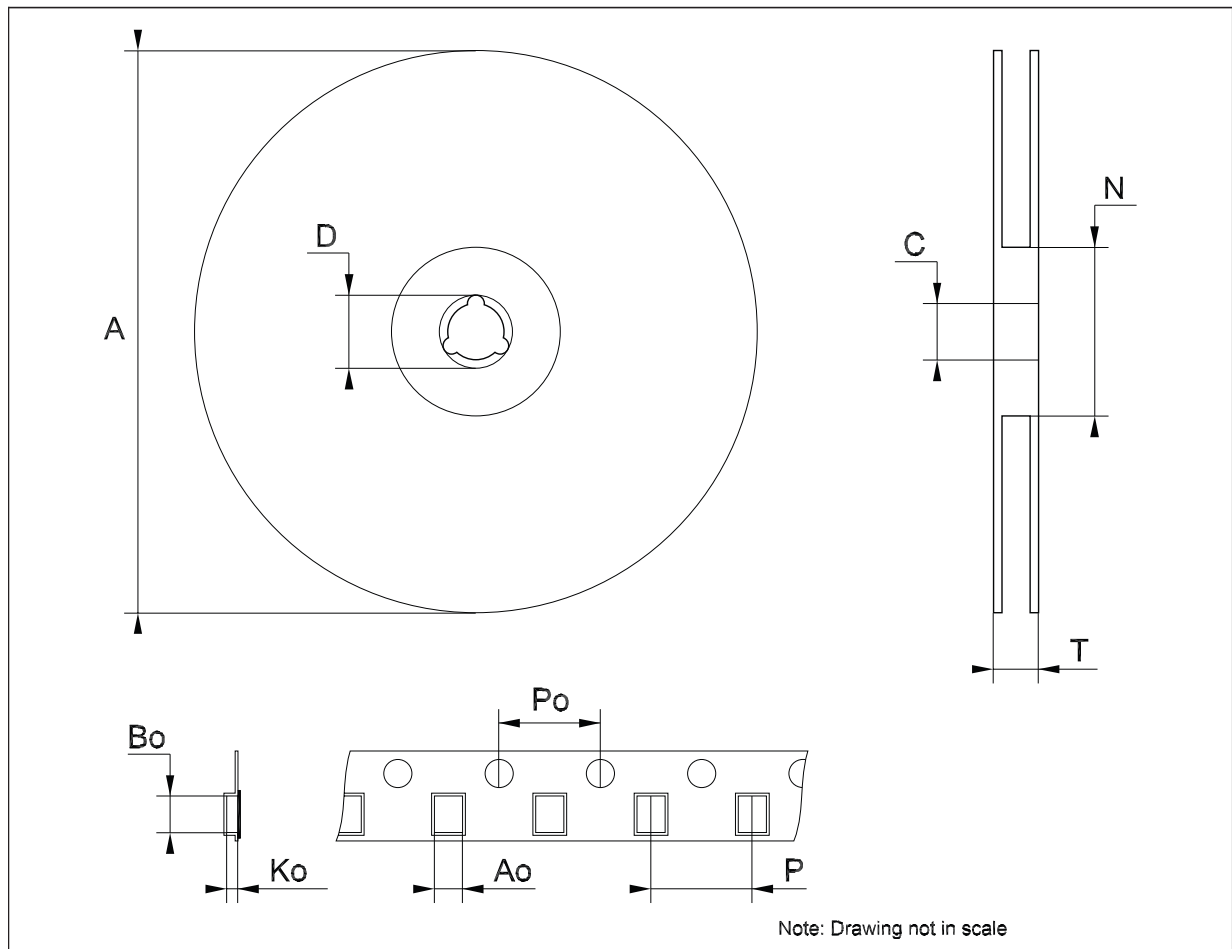
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23		0.45	0.009		0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23		2.50	0.088		0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.75	0.059		0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020





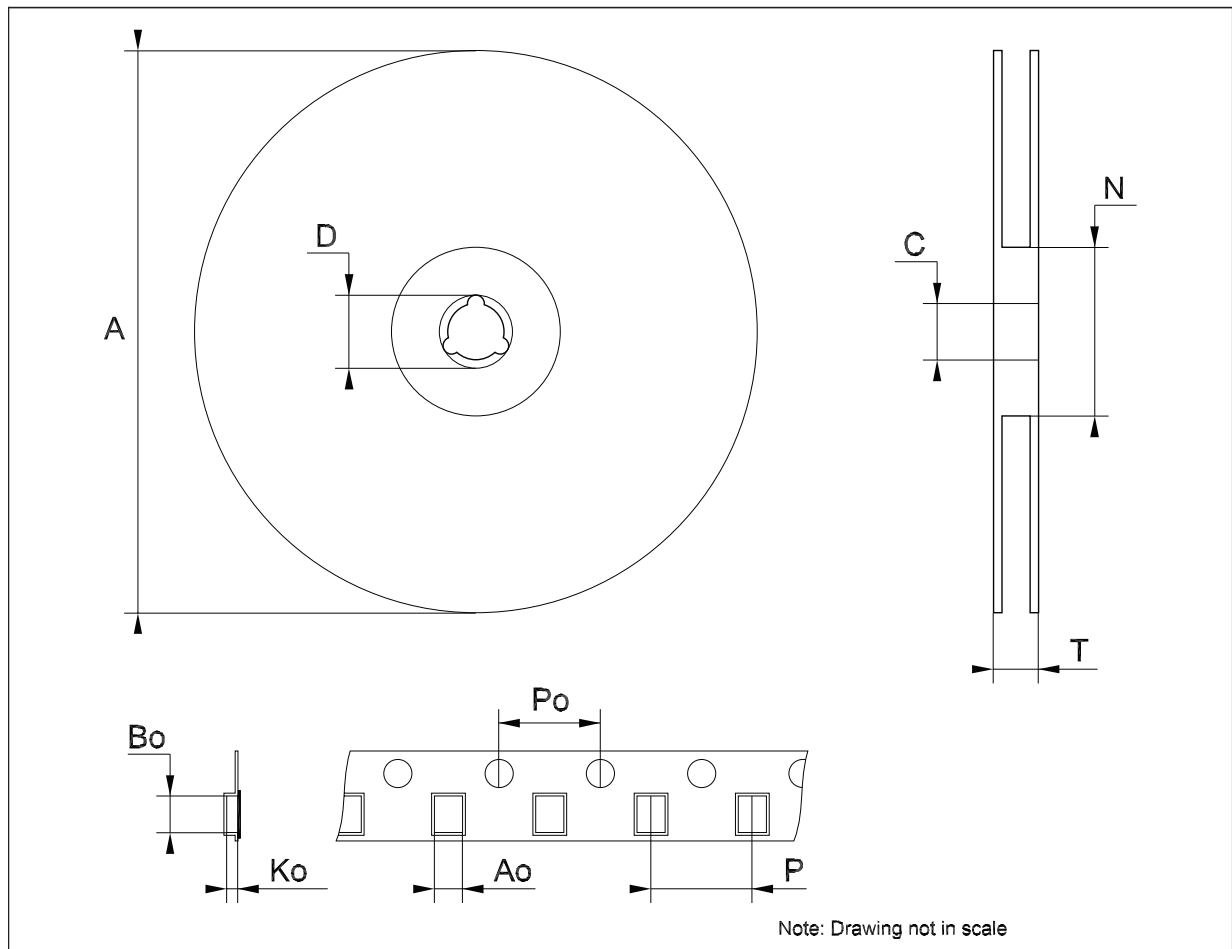
**Tape & reel SOT23-xL mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



**Tape & reel QFNxx/DFNxx (3x3) mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.087
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



## 8 Order codes

Table 6. Order codes

Packages				Output voltage
SOT23-5L	TSOT23	DFN6	DFN6D	
LDS3985M125R <sup>(1)</sup>		LDS3985PM12R <sup>(1)</sup>		1.25 V
LDS3985M135R <sup>(1)</sup>		LDS3985PM13R <sup>(1)</sup>		1.35 V
LDS3985M15R		LDS3985PM15R <sup>(1)</sup>	LDS3985PU15R	1.5 V
LDS3985M18R		LDS3985PM18R		1.8 V
	LDS3985G19R <sup>(1)</sup>			1.9 V
LDS3985M20R <sup>(1)</sup>		LDS3985PM20R <sup>(1)</sup>		2.0 V
LDS3985M21R <sup>(1)</sup>		LDS3985PM21R <sup>(1)</sup>		2.1 V
LDS3985M22R <sup>(1)</sup>		LDS3985PM22R <sup>(1)</sup>		2.2 V
LDS3985M25R		LDS3985PM25R		2.5 V
LDS3985M26R <sup>(1)</sup>		LDS3985PM26R <sup>(1)</sup>		2.6 V
LDS3985M27R <sup>(1)</sup>		LDS3985PM27R <sup>(1)</sup>		2.7 V
LDS3985M28R			LDS3985PU28R	2.8 V
LDS3985M285R <sup>(1)</sup>		LDS3985PM285R <sup>(1)</sup>		2.85 V
LDS3985M29R <sup>(1)</sup>		LDS3985PM29R <sup>(1)</sup>		2.9 V
LDS3985M30R		LDS3985PM30R <sup>(1)</sup>		3.0 V
		LDS3985PM31R <sup>(1)</sup>		3.1 V
LDS3985M32R <sup>(1)</sup>		LDS3985PM32R <sup>(1)</sup>		3.2 V
LDS3985M33R			LDS3985PU33R	3.3 V
LDS3985M47R <sup>(1)</sup>		LDS3985PM47R <sup>(1)</sup>		4.7 V
LDS3985M48R <sup>(1)</sup>		LDS3985PM48R <sup>(1)</sup>		4.8 V
LDS3985M49R <sup>(1)</sup>		LDS3985PM49R <sup>(1)</sup>		4.9 V
LDS3985M50R <sup>(1)</sup>		LDS3985PM50R <sup>(1)</sup>		5.0 V

1. Available on request.

## 9 Revision history

**Table 7. Document revision history**

Date	Revision	Changes
02-Dec-2004	1	First release.
10-Apr-2007	2	Added: new package TSOT23-5L.
16-May-2007	3	Added: new mechanical data DFN6D and order codes updated.
06-Sep-2007	4	Added: <a href="#">Table 1</a> in cover page.
11-Jun-2008	5	Modified: <a href="#">Table 6 on page 19</a> .

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